Remarks/Arguments

In the non-final Office Action mailed on 14 June 2004, the Examiner attempted to clarify his withdrawal of some previous prior art based rejections and apparently stated a new rejection (based in essence on an earlier rejection) rejecting all remaining claims 1, 2, 5-8, and 11-14 under 35 U.S.C. §103(a) as unpatentable over Ito (United States Patent Number 6,408,359) in view of Otterness (United States Patent Number 6,654,831) in further view of D'Errico (United States Patent Number 6,314,503).

Applicants respectfully traverse all remaining rejections. Applicants have amended remaining independent claims 1, 8, 13 and 14 for editorial clarity and to better protect the invention. Applicants respectfully request reconsideration and withdrawal of outstanding rejection of all remaining claims.

Remaining Rejections

Applicants continue to express concern over lack of clarity in the Examiner's position. In the Applicants' response of 21 April 2004 (in response to the Final Office Action mailed 27 February 2004), Applicants sought clarification as to which of the original four rejections were maintained (from the first Office Action mailed 8 September 2003) and attempted to respond to six new combinations of prior art used as a basis for rejecting various groups of claims.

In this new Office Action mailed 14 June 2004, the Examiner clarifies that all of the original four bases for rejection were intended to be withdrawn by the Final Office Action (see Office Action of 14 June 2004 at p. 2). Next the Examiner clarifies that the Final Office Action intended to state six new combinations as bases for rejection of various groups of claims (see Office Action of 14 June 2004 at p. 2-3). The Examiner then recites five of the six bases for rejection as now withdrawn (see Office Action of 14 June 2004 at p. 3). The Examiner apparently does not withdraw the rejection of claims 1, 2, 5-8 and 11-13 under 35 U.S.C. §103 as unpatentable over Ito in view of Otterness. Without further comment on that remaining earlier rejection, the Examiner apparently states a new rejection of claims 1, 2, 5-8 and 11-14 under 35 U.S.C. §103 as unpatentable over the combination of Ito, Otterness and D'Errico. In his "Response to Amendment" at

page 13 of the Office Action of 14 June 2004, the Examiner then states that all previous §103 rejections are withdrawn and repeats only the new rejection based on the combination of Ito, Otterness and D'Errico.

A new rejection of claims 1, 2, 5-8 and 11-14 over the combination of Ito, Otterness and D'Errico would logically subsume the earlier rejection of claims 1, 2, 5-8 and 11-13 (excluding claim 14) over the combination of Ito and Otterness (without D'Errico). Therefore, despite the confusion in the Examiner's statements, Applicants assume that the Examiner intended to withdraw ***ALL*** previous prior art based rejections and to recite only a new rejection based on the combination of Ito, Otterness and D'Errico.

Adding further confusion, in the body text of the new rejection of claim 1, for example, on pages 2-7 the Examiner intermingles argument paragraphs labeled "(Previous Action)" with other paragraphs labeled "(NEW)". On page 7, the Examiner begins mixing together rejection arguments for claim 1 with those related to claim 8 – in the middle of his discussion regarding the rejection of claim 1. In particular, on page 7, the Examiner remarks regarding an issue directed solely to claim 8. The very next paragraph on the top of page 8 continuing through page 10 then resumes his discussion of the basis for rejection of claim 1 again mixed with some arguments relating to both claims 1 and 8 or relating to claims 1, 8 and 14. This organization is, to say the least, confusing.

Despite this confusion in the Office Action, Applicants have attempted to respond as best they can to the Examiner's rejection of claims 1, 2, 5-8 and 11-14 under 35 U.S.C. §103 as unpatentable over Ito in view of Otterness further in view of D'Errico.

Section 103 Rejection

The Examiner rejected all remaining claims 1, 2, 5-18 and 11-14 under §103 as unpatentable over the combination of Ito, Otterness and D'Errico. The Examiner appears to suggest that some portions of Ito, Otterness and/or D'Errico teach essentially every element of the rejected independent claims 1, 8, 13 and 14 – though it is difficult to

identify in the Examiner's remarks precisely what the differences are between the proposed prior art combination and the rejected claims.

One aspect that appears clear in the Examiner's rejection of all independent claims (1, 8, 13 and 14) is that the Examiner is broadly defining a "host device" such that he apparently finds the requisite communication between the CSA (consolidated storage array) and the host device as the Examiner reads the term. In particular, the Examiner makes a point of reading the "host device" in Ito as the "external device, which can run software applications for Video-On-Demand service (column 1, lines 21-24)." While such a video server may be understood, generally, as a host device, it does not provide the recited relationship with the CSA (nor is such an operational relationship inherent in any host device/CSA interaction).

The recited "host device" should be clearly understood in the rejected claims and throughout the supporting specification as a computing system on which storage management processes and application processes are operable (e.g., host-based striping software, data access software, etc.). The host-based striping or data access is performed at a host device level because the CSA comprises a plurality of storage arrays – each storage array a substantially self-contained subsystem operable substantially independent of all other storage arrays. Under the invention of the rejected claims, the storage arrays cannot themselves (collectively or individually), stripe or access data of the logical volume distributed over the plurality of storage arrays – the storage arrays simply do not communicate with one another with such information. Only the host-based striping or data access software operable on the host device may properly communicate with each of the plurality of substantially independent storage arrays to effectuate the desired manipulation of data distributed over the plurality of independent arrays.

To effectuate such host-based striping or access to data on a logical volume, the host-based software ***must be*** aware of the ultimate configuration of the plurality of storage arrays used by the CSA to create the logical volume. No such knowledge of the storage arrays selected to store the logical volume is required in the teachings of Ito, Otterness, D'Errico or any other prior art of record (considered individually or in any

combination). None of the prior art of record teaches or reasonably suggests communicating information regarding the logical volume back to the host device to configure the host-based data access or striping software. Rather, all prior art of record states or implies that the data is stored and mapped within the storage subsystem in a manner transparent to the host system. In other words, the host system is totally unaware of the mapping of data to multiple storage devices. There is no need to send volume information back to the host device to configure the host based software.

The Examiner suggests on page 7 that:

> It is inherent that once the virtual data volume is created among the storage arrays and the storage devices that the applications running on a host device, which sent the volume request to the system of Ito, would have used the allocated storage locations to store and retrieve data. Address position file (volume information) is sent from the consolidated storage array to the host device.

Such a feature not inherent in the operation of storage arrays. To the contrary, it is generally a hallmark of modern storage arrays that mapping of logical to physical locations for information storage is completely transparent to the attached host systems. The storage controllers of modern storage arrays re-locate and map host supplied logical addresses to any of multiple locations on multiple storage devices within the storage array.

The external device in Ito (video server) requests creation of a volume. The storage array structure of Ito determines a location for the requested volume based on various criteria supplied by the creation request. An address position file (read by the Examiner as "volume information") depicted as 2401 and 2402 in Ito's figure 7 is created to define the mapping of the logical addresses of the created logical volume. However, nothing in Ito or any of the prior art of record suggests that this file is sent to the external device in Ito. Nothing in Ito suggests that this "volume information" is sent to the host device nor even that the host device would have any use for such information. Rather, Ito is silent as to where the address position file is used and suggests nothing more than that which is well known in the storage arts – that the address position file is used ***within the storage array*** to map host supplied logical addresses to physical addresses. None of the

prior art of record, considered individually or in any combination, teaches or reasonably suggests that Ito's address position file need be sent to the host device for any reason whatsoever. Rather, by contrast, the prior art of record suggests only the well-known transparency feature of modern storage systems whereby the mapping of information (i.e., the striping, etc.) is performed completely within the storage subsystem with no knowledge of the host system and hence no volume information returned to the host to configure the data access or striping software. D'Errico, for example, clearly recites throughout that his mapping methods and structures are operable "transparent to the host computer" (see, e.g., Abstract). Such transparency to the mapping of data (e.g., the striping of data) within a storage array is axiomatic in modern storage systems. The need to communicate volume information back to the host device to configure the data access or striping software operable thereon arises only from the needs of a consolidated storage array – a collection of substantially independent storage arrays. Only the host device can effectuate the desired striping or data access over such a plurality of storage arrays.

Applicants have amended all independent claims 1, 8, 13 and 14 to clarify the nature of the interaction between a CSA and the host system/device. In particular, the claims as amended clarify that the host device is one on which system and application processes are operable to effectuate striping or data access configured in accordance with the volume information returned from the consolidated storage array.

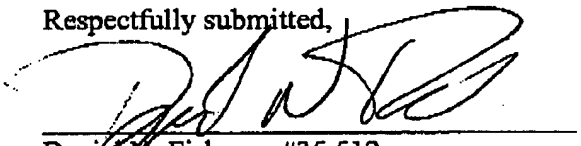
In view of the above discussion and the amendments to independent claims, remaining claims 1, 2, 5-8 and 11-14 are maintained to be allowable over all prior art of record, considered individually or in any combination. Applicants therefore respectfully request reconsideration and withdrawal of the rejection of all remaining claims (1, 2, 5-8 and 11-14).

Conclusion

Applicants have addressed all of the Examiner's outstanding rejections and have requested reconsideration and withdrawal of the outstanding rejections of remaining claims 1, 2, 5-8 and 11-14.

No additional fees are believed due. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,



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